

### **REMARKS**

The Office Action dated July 10, 2003, has been received and carefully noted. The amendments made herein together with the following remarks, and the attached Verified Translation of Japanese Patent Application No. H11-201875 are submitted as a full and complete response thereto.

Claim 1 has been amended. A replacement Figure 4 is respectfully submitted. Applicant submits that the amendments made herein are fully supported in the specification and the drawings as originally filed, and therefore no new matter has been added. Accordingly, claims 1-6 are pending in the present application and are respectfully submitted for consideration.

The drawings were objected to because Figure 4 should be designated by a legend such as --Prior Art--. Applicant respectfully presents herewith replacement Figure 4 which include the desired changes, without markings, and which comply with §1.84. Figure 4 has been amended to include a legend of --Prior Art--. Applicant respectfully requests consideration of amended Figure 4.

Claim 1 was objected as containing a minor informality therein. Applicant submits that claim 1 has been amended to correct the minor informality, and it is submitted that the amendment to claim 1 does not narrow the scope of the claim. Accordingly, Applicant submits that claims 1-6 are in full compliance with US patent practice.

Claims 1-6 were rejected under 35 U.S.C § 102(e) as being unpatentable over Kim (U.S. Patent No. 6,462,378). Applicant respectfully traverses this rejection and submits the attached verified translation of the priority document.

It is submitted that the filing of the attached verified translation perfects the claim of priority of the present application to the priority date of July 15, 1999 which predates the filing date of Kim. Therefore, Applicant submits that Kim is an improper reference under 35 U.S.C. § 102(e).

Specifically, it is submitted that Kim is an invalid reference because the present application was filed in the USPTO on January 14, 2002, in which the Applicant claims priority to Japanese Patent Application No. H11-201875 filed July 15, 1999. Therefore, the present application has an effective filing data of July 15, 1999.

In addition, the Office Action dated July 10, 2003 acknowledges that a claim of priority was made under 35 U.S.C. § 119(a)-(d) or (f).

Also, the effective filing date of Kim under 35 U.S.C. § 102(e) is the U.S. filing date, that being October 27, 1999.

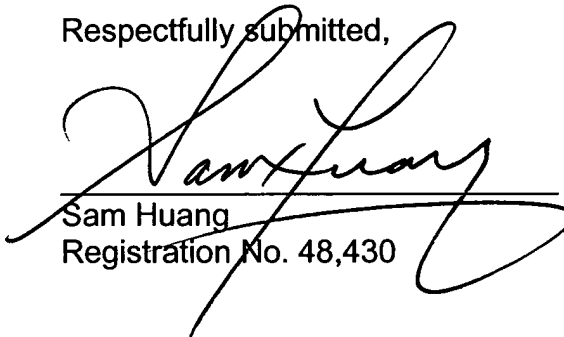
Given that the effective filing data of the present application (July 15, 1999) precedes the effective filing date of Kim (October 27, 1999), Applicant submits that Kim is not a valid reference under 35 U.S.C. § 102(e) based on the verified translation of the priority document filed with the USPTO.

In view of the above, Applicants respectfully submit that each of claims 1-6 recites subject matter that is novel and new, and therefore respectfully requests that claims 1-6 be found allowable and that this application be passed to issue.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the Applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper has not been timely filed, the Applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300 referring to attorney docket number 107400-00045.

Respectfully submitted,

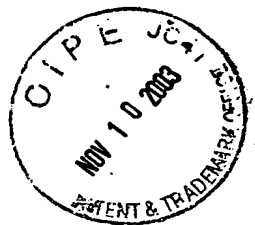


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Enclosures: Petition for Extension of Time (1 month)  
Verified Translation Document  
Replacement Figure 4



VERIFICATION OF TRANSLATION

I, Kiyoshi Kawamura, being a citizen of Japan, residing at c/o KAWAMURA & CO., Shinei Bldg. 6E, 5-1, Nishinakajima 4-chome, Yodogawa-ku, Osaka-shi, Japan, do solemnly and sincerely declare as follows:

I am a translator, of KAWAMURA & CO., of Shinei Bldg. 6E, 5-1, Nishinakajima 4-chome, Yodogawa-ku, Osaka, 532-0011, Japan.

I am well acquainted with the English and Japanese languages.

The attached translation is a true and correct translation into the English language of a certified copy of Japanese Patent Application No. 201875/1999 filed on July 15, 1999.

I declare further that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment.

This 4th day of November, 2003

by Kiyoshi Kawamura  
Kiyoshi Kawamura

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Patent Application Hei. 11-201875

[Name of Documents] Application for Patent

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[Filling Date] July 15, 1999

[Addressee] Commissioner of the Patent Office

[IPC] H01L 29/70

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[Indication of Charge]

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Patent Application Hei. 11-201875

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[Name of Item] Specification 1

[Name of Item] Drawings 1

[Name of Item] Abstract 1

[General Power of Attorney No.] 9401527

[Proof] Necessary

[Document Name] SPECIFICATION

[Title of the Invention] SEMICONDUCTOR DEVICE

[What is claimed is:]

[Claim 1] A semiconductor device having a MOS type field effect transistor comprising a built-in diode incorporating a universal junction structure,

wherein said diode forms a current path between a source and a drain, when said MOS field effect transistor turns off.

[Claim 2] The semiconductor device of claim 1, wherein said universal junction structure is formed in a surface region of a semiconductor substrate.

[Claim 3] The semiconductor device of claim 1 or 2, wherein said universal junction structure is connected to a source electrode or drain electrode.

[DETAILED DESCRIPTION OF THE INVENTION]

[0001]

[Field of the Invention]

The present invention relates to a semiconductor device having a MOS field-effect transistor such as a power MOSFET.

[0002]

[Prior Art]

A driver circuit is frequently used which employs a MOSFET to drive an inductive load such as a motor. For example, the power MOSFET has such a configuration, that a P-well is formed on the surface of an N-type semiconductor layer provided on a N<sup>+</sup>-type semiconductor substrate, and at this

P-well is formed a ring-shaped  $N^+$ -type source diffusion layer. In this configuration, the semiconductor substrate outside the P-well acts as a drain layer. On the surface region of the P-well a gate electrode is provided through a gate insulator film. Thus, the MOSFET is formed.

[0003]

A PN junction of the P-well and the N-type semiconductor layer forms a so-called built-in diode (body diode). This built-in diode can be used as a flywheel diode for inducing a reverse recovery current ascribed to a counter electromotive force of an inductive load.

[0004]

[Problem to be solved by the Invention]

The counter electromotive force of the inductive load acts to apply a voltage in the forward direction on the built-in diode, which is accompanied, as well known, by accumulation of minority carrier, that is, electrons in the P-well. Thus accumulated minority carrier inhibits rapid interruption of the operation of the built-in diode at the time of rectification when the current is changed in flow direction. Moreover, if the flow of this minority carrier is concentrated to part of the device, the PN junction portion of the P-well and the drain layer is broken and hence the power MOSFET is broken eventually.

[0005]

In view of the above, it is an object of the invention to provide a semiconductor device including a MOSFET that



can solve these technological problems in providing high-speed switching operations and improving the breakdown resistance amount (withstanding voltage).

[0006]

[Means to solve the Problems and effect of the invention]

The invention referred in claim 1 is a semiconductor device having MOS type field effect transistor, characterized in that a built-in diode is provided in MOSFET, which has a universal junction structure and forms a current path between a source and a drain, when the above MOSFET turns off.

[0007]

More specifically, the above MOS field effect transistor includes; a well having a first conductivity type formed in a semiconductor substrate, a source region having a second conductivity type (which is different conductivity type from the first conductivity type) formed in the well, and a drain region having a second conductivity type formed in contact with the well, wherein the built-in diode may be formed by PN junction between the well and the drain region. In this case, it is preferable that the universal junction structure is provided such that it is in contact with the source electrode on a surface of the well.

[0008]

The universal junction structure is configured in such that first regions which act as barriers for minority carrier in the well, and second regions which take in the minority

carrier are arranged alternately in a cross direction to the moving direction of charges. It is preferable that the source electrode is provided so as to contact to the first and second regions. For example, when the well is P-type region, P<sup>+</sup>-type regions and N<sup>+</sup>-type regions are arranged alternately in a cross direction to the moving direction of charges, or P<sup>+</sup>-type regions and P-type regions are arranged alternately in a cross direction to the moving direction of charges. Such configuration forms the universal junction structure.

[0009]

By this construction, the accumulation of the minority carrier in one region of the built-in diode (for example, the P-well) is suppressed, because the universal junction structure is incorporated in the built-in diode. This mechanism enables rapidly not to make a working of the built-in diode. Also, since the minority carrier is not accumulated, a large current is not concentrated to part of the device at the time of rectification, thus enabling enhancing the withstanding voltage.

[0010]

The invention of claim 2 is the semiconductor device according to claim 1, wherein the universal junction structure is formed in a surface region of a semiconductor substrate.

By this structure, the universal junction structure is easily formed, and joining the universal junction

structure to an electrode (source electrode or drain electrode) is easily obtained.

[0011]

The invention of claim 3 is the semiconductor device according to claim 1 or 2, wherein the universal junction structure is connected to a source electrode or drain electrode.

By this structure, the minority carrier dropped in the universal junction structure is instantly taken in to prevent the minority carrier accumulating.

[0012]

[Embodiments of the Invention]

The following will describe a semiconductor device having a MOSFET according to the present invention with reference to the drawings. As can be seen from its cross-sectional view of one embodiment shown in FIG. 1, in a semiconductor device having a MOSFET of the present invention, in a surface of the N-type semiconductor layer 20 is formed a predetermined pattern of a P-wells 21. For example, directly below a gate pad 36 to which a gate terminal 35 is connected, a large-area P-well 21 (P-well below the pad) is formed, and in the remaining region is formed an evenly spaced plurality of the P-wells 21 in a matrix pattern, and each of P-wells 21 is, for example, rectangular in a plan view.

[0013]

At each of the P-wells 21 is formed, for example, a

rectangular ring-shaped  $N^+$ -type diffused source region 22. The semiconductor substrate 20 except this P-well 21 and an  $N^+$ -type region 23 on a rear surface of the semiconductor substrate 20 acts as a drain region 25, thus providing a vertical-type double-diffusion MOSFET. On the  $N^+$ -type region 23 is provided a drain electrode 24.

[0014]

In the P-well 21, a surface layer portion positioned between the drain region 25 and the diffused source region 22 provides a channel region 26 in which is formed a channel 50 when the MOSFET is turned ON. Above this channel region 26 is formed a gate electrode 28 with a gate insulator film 27 interposed therebetween. The gate electrode 28 directly below the gate pad 36 is connected to the gate pad 36 through a contact hole 30 formed in the insulator film 29 on the gate electrode 28. The other gate electrodes 28 are connected to the gate electrodes 28 directly below the gate pad 36 at a position not shown in the figure.

[0015]

In the insulator film 29 are formed, on the surface of each P-well 21, a source contact hole 31 for exposing the diffused source region 22 provided in this P-well 21 and the surface of the P-well 21 surrounded by this diffused source region 22. A source electrode 33 formed on the insulator film 29 is commonly connected through this source contact holes 31 to all of the diffused source region 22 provided on the semiconductor substrate 21 and the surfaces

of portions surrounded by the diffused source region 22 in each P-well 21.

[0016]

In a PN junction between P-type well 21 and N-type drain region 25, a built-in diode D that becomes conductive when a voltage in the reverse direction to that applied when this MOSFET is operated is formed. That is, this built-in diode D may be used as a flywheel diode for flowing therethrough a reverse recovery current ascribed to a reverse electromotive force of an inductive load such as a motor when this MOSFET is used to drive it.

[0017]

The universal junction structure 40 is provided in all P-type wells including P-type well 21 under electrode pad, to develop the operation velocity (especially shut down velocity) of the built-in diode D, and to prevent large current flowing into PN junction of the built-in diode D. That is, the universal junction structure 40 is incorporated in the P-well 21 constituting the built-in diode D. This universal junction structure is provided in a region surrounded by source regions 22 on a surface of each P-type well 21, and it is connected to a source electrode 33.

[0018]

FIG. 2 illustrates an expanded view of the universal junction structure 40, FIG. 2(a) shows a plan view with removing the source electrode 33 etc. and FIG. 2(c) illustrates a partial expanded cross-sectional view. In

the outer surface layer of such a region of the P-well 21 that is surrounded by the rectangular ring-shaped diffused source region 22 are formed concentrically a small-width  $N^+$ -type (or N-type) ring-shaped region 41 and an equivalently small-width  $P^+$ -type (or P-type) ring-shaped region alternately. These regions 41 and 42 all come in contact with the source electrode 33. That is, the  $N^+$ -type region 41 and the  $P^+$ -type region 42 are arrayed alternately in a plan view along with a cross direction to the moving direction of charges.

[0019]

In such a configuration, electrons, if any as a minority carrier in the P-well 21, fall in the  $N^+$ -type region 41 and then can be drawn out to the source electrode 33 rapidly. Thus, it is possible to suppress the accumulation of electrons in the P-well 21.

When the MOSFET according to this embodiment is used to drive an inductive load such as a motor, a turn-ON voltage is applied at the gate electrode 28 to form a channel 50 (see FIG. 1) to thereby interconnect the source region 22 and the drain region 23 therethrough. When the MOSFET is ON, it turns out as a voltage in the reverse direction is applied on the built-in diode D.

[0020]

When a turn-OFF voltage is applied at the gate to give a non-conductive state between the source and drain regions, a reverse electromotive force is applied from the inductive

load to apply a voltage in the forward direction to the built-in diode D. In this case, a minority carrier (electrons in an example shown in FIG. 1) appears in the P-well 21, these electrons can fall into the  $N^+$ -type region and then be drawn out to the source electrode by the universal junction structure 40.

[0021]

Thus, when the MOSFET is turned ON, so that at the time of commutation (when such a situation occurs that a voltage in the reverse direction is applied to the built-in diode), the built-in diode D can be immediately blocked (turned OFF), thus shortening the reverse recovery time ( $t_{rr}$ ) significantly. Besides, no electrons are accumulated in the P-well 21, so that no large current is concentrated during commutation nor is destroyed the PN junction of the built-in diode D. These features enable manufacturing such a MOSFET that has significantly improved breakdown resistance amount as compared to that of the prior art construction.

[0022]

Specifically, the reverse recovery time  $t_{rr}$  of the built-in diode D could be shortened by about 30% and the avalanche current (largest current that does not destroy the PN junction) of the built-in diode D could be increased by about 20%.

FIG. 3 is a cross-sectional view for showing another configuration example of the universal junction structure 40. In FIG. 3, the same elements as those in FIGS. 1 and

2 are indicated by the same reference numerals. In this example, the universal junction structure 60 is comprised of a plurality of evenly spaced  $P^+$ -type regions 61. And a Schottky junction is formed between a source electrode 33 and the P-well 21 to thereby form Schottky universal junction structure in a region between adjacent  $P^+$ -type regions 61.

[0023]

In this construction, the minority carrier in the P-well 21 is rapidly released through the Schottky junction portion. This structure achieves the same effects as shown in FIG. 2.

Even though only one  $P^+$ -type region, or  $N^+$ -type or N-type region which is connected to the source electrode 33, is formed in a region surrounded by source regions, the universal junction structure according to the present invention is available. In this case, electrons in P-type well 21 are dropped in the universal junction structure to thereby be taken out by the source electrode 33.

[0024]

Although one embodiment of the invention has been described, the invention is applicable also to other embodiments. For example, although the above-mentioned embodiment has employed an N-channel type MOSFET, the present invention is applicable also to a P-channel type MOSFET. In this case, for example, an  $N^+$  region and a  $P^+$  region may be arrayed alternately in an N-well to provide a universal



junction structure, or a plurality of  $N^+$  regions are evenly spaced to provide a Schottky universal junction structure. In the Schottky junction portion in such a case, some of the electrode materials for the source electrode 33 may be made of Titanium (Ti) or Molybdenum (Mo) in place of Aluminum (Al).

[0025]

Also, the impurity-diffused regions which make up the universal junction structure need not be formed concentrically but may be formed in a straight stripe or any other appropriate shape. For example, when the P-well is formed in a stripe shape and source regions are also formed in a stripe shape therein, preferably the universal junction structure is formed in a stripe shape correspondingly.

[0026]

Further, although the above-mentioned embodiment has exemplified such a semiconductor device that has one MOSFET, the invention is applicable also to such a semiconductor device that has a plurality of MOSFETs or that a functional element other than a MOSFET on the same semiconductor substrate.

[BRIEF DESCRIPTION OF THE DRAWINGS]

[Fig. 1]

FIG. 1 is an expanded perspective and partial cross-sectional view for showing a construction of a MOSFET according to one embodiment of the present invention.

[Fig. 2]

FIG. 2 is a view showing one example of an expanded universal junction structure.

[Fig. 3]

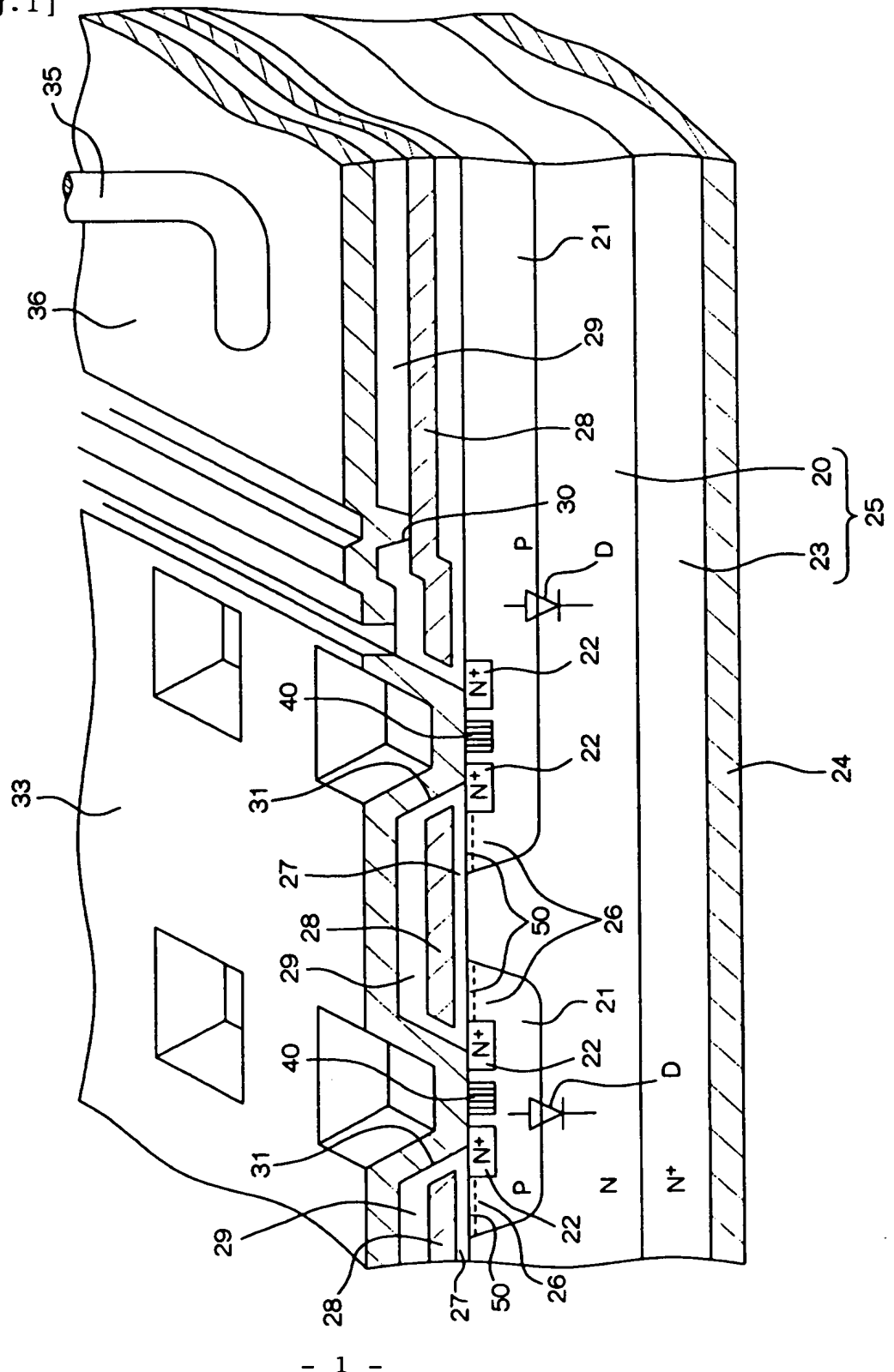
FIG. 3 is a view showing another example of an expanded universal junction structure.

[Explanation of reference characters]

20	N-type semiconductor substrate
21	P-type well
22	N <sup>+</sup> -type diffused source region
23	N <sup>+</sup> -type region
24	drain electrode
25	drain region
26	channel region
27	gate insulator film
28	gate electrode
33	source electrode
36	gate pad
40	universal junction structure
41	N <sup>+</sup> -type region
42	P <sup>+</sup> -type region
60	universal junction structure
61	P <sup>+</sup> -type region

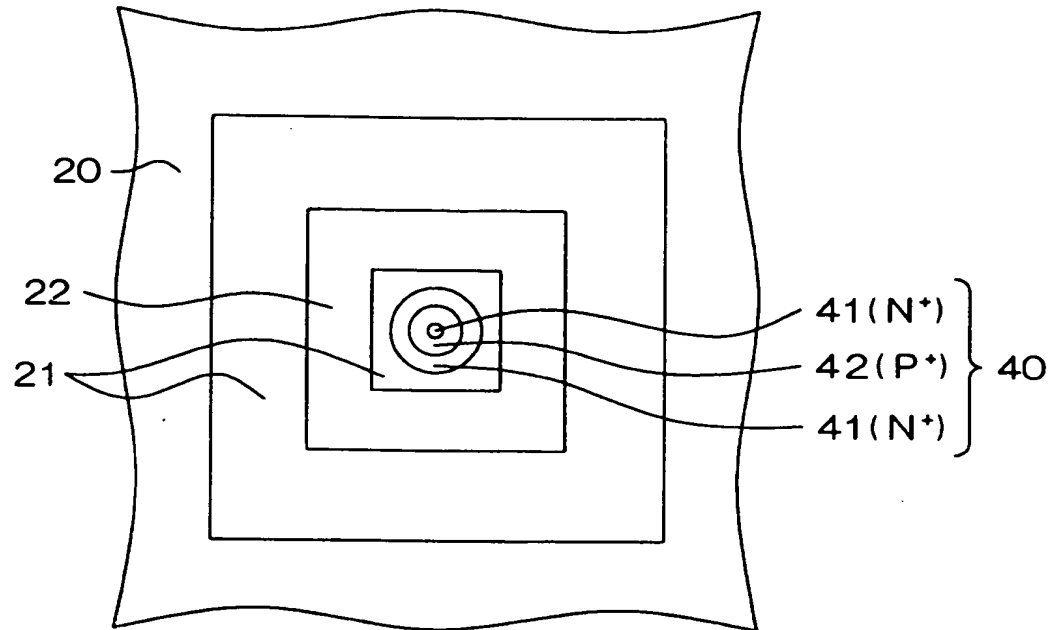
[Document Name] DRAWINGS

[Fig.1]

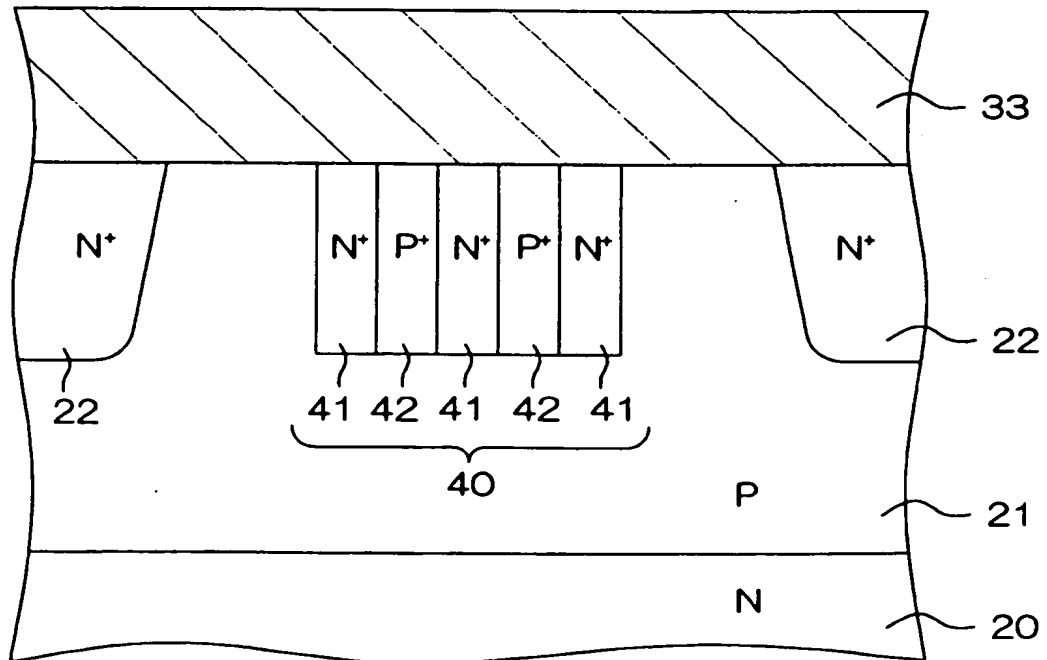


[Fig.2]

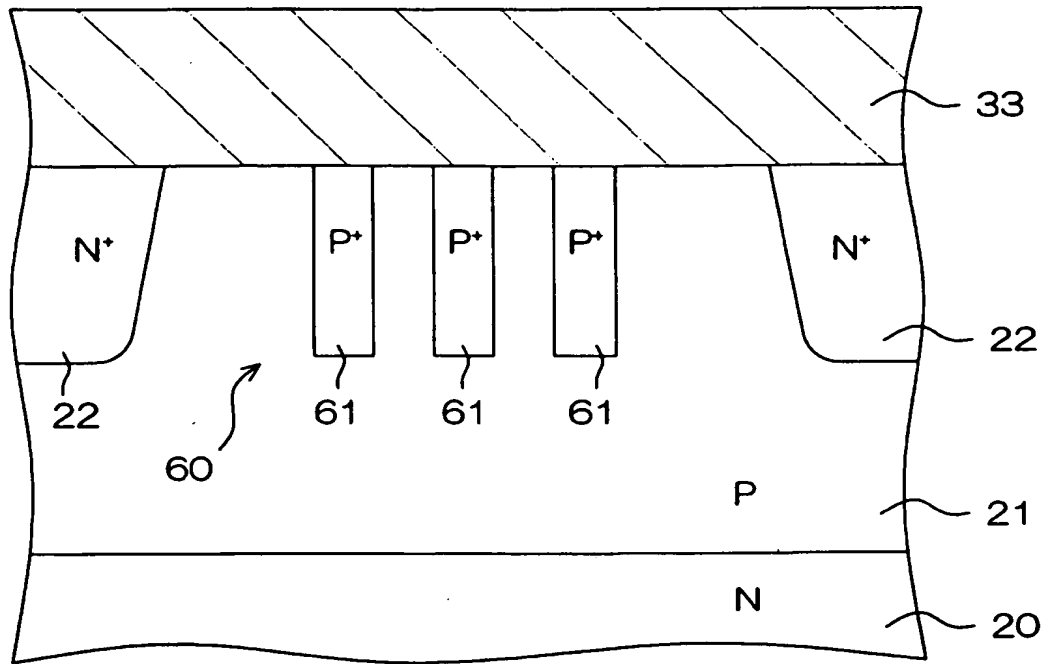
(a)



(b)



[Fig.3]



[Document Name] ABSTRACT

[Abstract]

[Purpose] Providing high-speed switching operations of a built-in diode incorporating in MOS field effect transistor, and improving the breakdown resistance amount.

[Solving Means] P-well 21 is formed in an N-type semiconductor substrate 20. N<sup>+</sup>-type source region is formed in the P-well 21. A universal junction structure 40 is provided in the P-well 21. This universal junction structure is connected to a source electrode 33. A PN junction between the P-well 21 and the N-type semiconductor substrate 21 constitutes a built-in diode D. When a forward voltage is applied to the built-in diode D, the minority carrier (electrons) arisen in the P-well 21 falls into the universal junction structure 40, thereby to be taken out to rapidly the source electrode 33.

[Figure Selected] Fig. 1